

CLAIMS

1. A package lid for attaching to a package substrate of a packaged semiconductor comprising:

a sloped wall configured to provide an exposed perimeter portion of the package substrate when the package lid is disposed on the package substrate to allow application of a molding compound on the exposed perimeter portion of the package substrate, the molding compound contacting the sloped wall to secure the package lid to the package substrate of the packaged semiconductor.

2. The package lid of claim 1 wherein the sloped wall has a slope angle between 30 degrees and 60 degrees.

3. The package lid of claim 1 further comprising a foot around at least a portion of the perimeter of the sloped wall, configured to contact the package substrate when the package lid is placed on the package substrate.

4. The package lid of claim 1 wherein the package lid is a stamped package lid.

5. The package lid of claim 4 wherein the stamped package lid has a thickness less than 2.39 mm.

6. The package lid of claim 4 wherein the stamped package lid has a thickness of about 0.79 mm.

7. The package lid of claim 4 wherein the stamped package lid has a thickness between about 0.45 mm and about 2.39 mm.

8. The package lid of claim 6 wherein the stamped package lid comprises nickel-plated copper.

9. The package lid of claim 1 further comprising a vent.

10. The package lid of claim 9 wherein the vent is provided in a side of the package lid.

11. The package lid of claim 10 wherein the vent comprises a gap in the sloped wall.

12. The package lid of claim 1 further comprising a rim forming a vertical wall around a top of the package lid.

13. The package lid of claim 12 further comprising fiducial marks formed in the rim.

14. The package lid of claim 13 wherein fiducial marks are formed in corners of a rectangular package lid.

15. The package lid of claim 1 wherein the package lid is substantially rectangular.

16. The package lid of claim 15 wherein the lid covers a rectangular semiconductor integrated circuit a side at least 25.4 mm long.

17. The package lid of claim 4 wherein the stamped package lid is rectangular and covers a programmable logic device at least 25.4 mm long on a first side.

18. The package lid of claim 1 wherein the exposed perimeter portion of the package substrate comprises polymer material.

19. The package lid of claim 1 wherein the package lid is disposed on the package substrate to provide the exposed perimeter portion and further comprising:

first molding compound applied to a first portion of the exposed perimeter portion and contacting the sloped sidewall, and

second molding compound applied to a second portion of the exposed perimeter portion and contacting the sloped sidewall, wherein the first portion of the exposed perimeter portion is opposite the second portion of the exposed perimeter portion.

20. The package lid of claim 19 wherein the package substrate includes an organic resin.

21. The package lid of claim 19 wherein the package substrate includes a solder ball-grid array for connecting the packaged semiconductor to a printed circuit assembly.

22. A method of packaging a semiconductor integrated circuit comprising:

attaching the semiconductor integrated circuit to a package substrate;

placing a package lid having a sloped wall on the package substrate over the semiconductor IC to leave an exposed perimeter portion of the package substrate;

applying molding compound to the exposed perimeter portion of the package substrate and the sloped wall;

hardening the molding compound to attach the package lid to the package substrate to provide a packaged integrated circuit.

23. The method of claim 22 wherein the step of attaching the semiconductor integrated circuit to the package substrate comprises a first solder re-flow process of a first ball-grid array.

24. The method of claim 22 further comprising a step, after the step of hardening the molding compound to attach the package lid to the package substrate, of attaching the packaged integrated circuit to a printed circuit board using a second solder re-flow process of a second ball-grid array.

25. The method of claim 22 wherein the molding compound is applied in a plastic or fluid state.

26. The method of claim 22 further comprising a step, prior to the step of placing the package lid having the sloped wall on the package substrate over the semiconductor IC, of stamping the package lid out of metal.

27. The method of claim 26 wherein the metal comprises nickel-plated copper.

28. The method of claim 26 wherein the metal is less than 0.79 mm thick.

29. The method of claim 26 wherein the metal is about 0.79 mm thick.

30. The method of claim 22 wherein the exposed perimeter portion is about 1 mm wide.

31. A package lid for attaching to a package substrate for a packaged semiconductor comprising:

means for providing a sloped wall of the package lid;

means for providing an exposed perimeter portion of the package substrate; and

means for securing the package lid to the package substrate contacting the sloped wall of the package lid and the exposed perimeter portion of the package substrate.